THE TELETEK SBC 86/87

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Teletek's SBC 86/87 is a 16-bit slave single board computer intended for use on the S-100 bus in a multiuser/multiprocessing system. This slave board gives the system integrator the flexibility of mixing 8-bit economy with 16-bit processing power.

Since the SBC 86/87 is designed as an I/O mapped slave on the S-100 bus, it can be added to any existing S-100 system to expand the processing capability. In the following pages, I will introduce the features of this slave SBC and show how it interfaces to an existing S-100 bus system.

DESIGN PHILOSOPHY

The SBC 86/87 was designed to provide an easy-to-implement 16-bit alternative for system integrators. With this board, the integrator can provide 16-bit, high-speed performance where required in a system, and yet retain the cost-effectiveness of 8-bit SBCs for system functions that do not need the additional capability. With the addition of this slave to an existing 8-bit system, the user can access CP/M-86 application software and the power of the 8087 math coprocessor for numeric intensive applications.

The interface to the S-100 bus was kept as simple as possible to allow this board to work with a variety of S-100 systems. All communications to and from the slave take place through two I/O mapped FIFO buffers. This greatly simplifies the requirements for the bus master.

THE CPU AND NPX

The SBC 86/87 utilizes the Intel 8086 CPU and the companion 8087 math coprocessor, both running at 8MHz. Since the SBC 86/87 operates independently of the S-100 bus, the internal speed can be different from that of the main system CPU.

The 8087 coprocessor adds arithmetic, trigonometric, exponential, and logarithmic instructions to the standard 8086 instruction set. The 8087 will significantly improve the performance of the CPU during numeric intensive operations. The 8087 coprocessor conforms to the proposed IEEE Floating Point Standard.

In addition to the 8087, this board design incorporates several other peripheral-support ICs that increase the capability of the slave SBC. These include an Intel 8208 DRAM controller, the Intel 8256 MUART, and the Signetics 2651 USART.

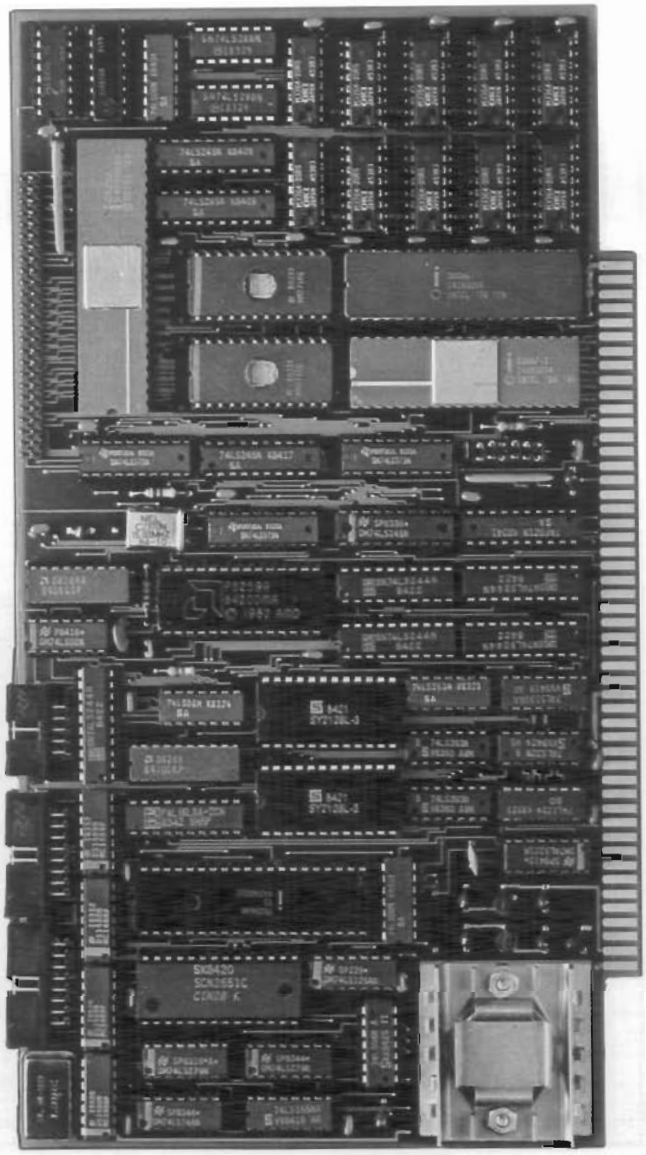
ON-BOARD MEMORY

The standard SBC 86/87 includes 128K bytes of RAM, expandable to 512K by using 256K-bit RAM ICs. The memory layout uses stacked RAM ICs to reduce the physical size of the array. The standard board also provides 4K bytes of EPROM using two 2716s. It is expandable to 64K bytes by using two 27256 EPROMs. Normally, the on-board EPROM contains hardware initialization and system-boot software.

The on-board RAM controller, an Intel 8208, supports either 64K or 256K devices. It generates the necessary signals to address, refresh, and directly drive the memory array. The controller is automatically initialized upon reset by a 74LS165 shift register. The 8208 controller allows operation without wait states when accessing

TELETEK SBC 86/87

USE:	S-100 16-bit slave SBC for use in TurboDOS multi-user/multiprocessing systems.
MANUFACTURER:	TELETEK ENTERPRISES, INC. 4600 Pell Drive Sacramento, CA 95838 (916) 920-4600
FEATURES:	Processor — 8086 16-bit, 8 MHz. Optional 8087 Math Coprocessor. Memory — 128K RAM (expandable to 512K using 256K DRAMs), 4K ROM (expandable to 64K), 4K FIFO. I/O — Two RS-232C serial ports, One Centronics compatible printer port.
SOFTWARE:	TurboDOS
MANUALS:	Technical Reference Manual, 31 pages.
PRICE:	$899 for 128K, w/o 8087 (100 quantity).



RAM memory, while a single wait state is inserted for each access of EPROM.

THE INTEL 8256 MUART

The 8256 is labeled as a Multi-Function Universal Asynchronous Receiver-Transmitter (MUART). As the name implies, this peripheral-support IC offers more than just a serial communications port inside its 40-pin DIP package. The extra functions include 16 bits of parallel I/O, five 8-bit counter/timers, and an eight-level priority interrupt controller.

The asynchronous serial communications port provides one of the two RS-232C compatible serial ports on the SBC 86/87. (The other is generated by the Signetics 2651 USART.) To permit a variety of operating speeds without additional external components, the MUART serial port includes an internal software programmable baud rate generator. This serial port can be programmed by the CPU for different character sizes, parity generation and detection, error detection, and start/stop bit handling. The line drivers and receivers are supplied on board of the SBC 86/87, eliminating the requirement for "paddle boards" on the peripheral cables.

A Centronics-compatible printer port is derived from the two parallel ports on the 8256. One parallel port is responsible for the printer data lines and a portion of the other for the printer control signals. The remaining signals of the second parallel port are used in the interrupt circuit. They also provide optional control lines for the MUART serial interface. The cable line drivers for the Centronics port are also included on board.

The five 8-bit timing channels furnished by the MUART can also be used for event counting. Additionally, four of the channels can be cascaded into two 16-bit counter/timers if desired. The clock source for these circuits comes from the 5.0688 MHz oscillator used with the 2651 USART.

The SBC 86/87 supplies two cascaded eight-level Priority Interrupt Controllers (PICs) to resolve all on-board and bus master interrupts. An Intel 8259A acts as the master PIC. The second PIC is provided by the 8256 MUART.

Table 1 shows the PIC assignments as well as the Non-Maskable Interrupt (NMI) assignment.

8259A PIC

Number	Usage
NMI	Memory Parity Error
0	MUART
1	USART Transmit Buffer Empty
2	USART Receive Data Available
3	Tx INT from master
4	Rx INT from master
5	Aux. INT from master
6	8087 NPX
7	EXPANSION BUS

8256 MUART

Number	Usage
0	Timer 1
1	Timer 2 or Port 1 P17 Interrupt
2	External Interrupt (EXTINT)
3	Timer 3 or Timers 3 & 5
4	Receiver Interrupt
5	Transmitter Interrupt
6	Timer 4 or Timers 2 & 4
7	Timer 5 or Port 2 Handshaking

Table 1. *PIC and NMI assignments.*

THE 2651 USART

The 2651 combines, in a single 28-pin DIP package, the necessary features for a serial interface with a programmable baud rate generator. This allows the designer to conserve valuable board real estate for other functions. The baud rates are derived from an external clock oscillator, and their operation is independent of the MUART serial port. The 2651 serial interface provides full modem control signals. These signals support hardware handshaking protocols of peripheral devices that require them.

S-100 FIFO INTERFACE

All information other than protocol control signals, exchanged between the S-100 bus master and the SBC 86/87, occurs via the dual FIFO memory circuit on board the slave. One FIFO buffer is dedicated to receiving data from the S-100 master. The other is dedicated to sending data to the master. The SBC 86/87 cannot function as the bus master of a system. Therefore, it depends on a master processor to manage all the system data transfers through these I/O mapped buffers.

This method of system communication combines the simplicity of mapping the slaves as ports in the master I/O space with the high performance of using DMA block data transfers between the master memory and the slave FIFO buffer. Unlike a memory-mapped DMA system, where the slave's RAM is mapped into the master's memory space, the slave CPU does not have to be idle during the transfer. While the data transfers are taking place between the master processor and the FIFO, the slave processor is free to perform normal operations. Also, no complicated memory management capability is required of the bus master.

Asynchronous communication is inherent in the design of this type of system. The master processor and any SBC 86/87 slaves in the system operate independently of each other. In fact, the master processor and the slaves can be running at altogether different clock speeds.

MASTER/SLAVE COMMUNICATIONS

The SBC 86/87 appears as a cluster of four I/O ports to the bus master. By accessing these ports, the master can control data transfers between itself and the slave. Each SBC 86/87 has option jumpers that allow it to be addressed on any four-port boundary within the first 256 I/O locations. Table 2 illustrates how each port is used.

STATUS REGISTER

The status register contains three flags that can be set by the slave and read or cleared (by sending interrupts) by the master. This register is normally polled by the master during network communications over the S-100 bus. The diagram in Figure 1 illustrates how the status register is defined.

INTERRUPTS

The bus master can cause three different interrupts to the slave: the Rx INT, the Tx INT, and the Aux INT. Anytime one of these interrupts is sent to the slave by accessing the appropriate I/O port, the associated

flag in the status register is cleared.

The Rx INT is used to indicate to the slave that the master has written data to the slave RxFIFO. The Tx INT is used to indicate that the master has read data from the slave TxFIFO. The Aux INT and Aux flag, in the status register, are free for programmer defined functions. The most common usage is for a "slave running" check: the master sends an Aux INT to the slave, and the slave responds by setting the Aux flag in the status register.

port0	*input*	=	read from slave status register
	output	=	send Tx INT to slave, reset TxRDY flag to master
port1	*input*	=	read data from slave TxFIFO
	output	=	write data to slave RxFIFO
port2	*input*	=	send Aux INT to slave, reset Aux flag to master
	output	=	reset slave RxFIFO address counters
port3	*input*	=	reset the slave
	output	=	send Rx INT to slave, reset RxRDY flag to master

Table 2. *I/O Port Assignments.*

RESET

Two levels of reset are available on the SBC 86/87. The first is a system reset; all boards (and therefore all users) in the system are reset simultaneously by activating the RESET* signal (pin 75) on the S-100 bus. The second type of reset is a software reset; the master issues an I/O command to individually reset one user. This allows the master CPU to "wake up" a user that doesn't respond to an inquiry.

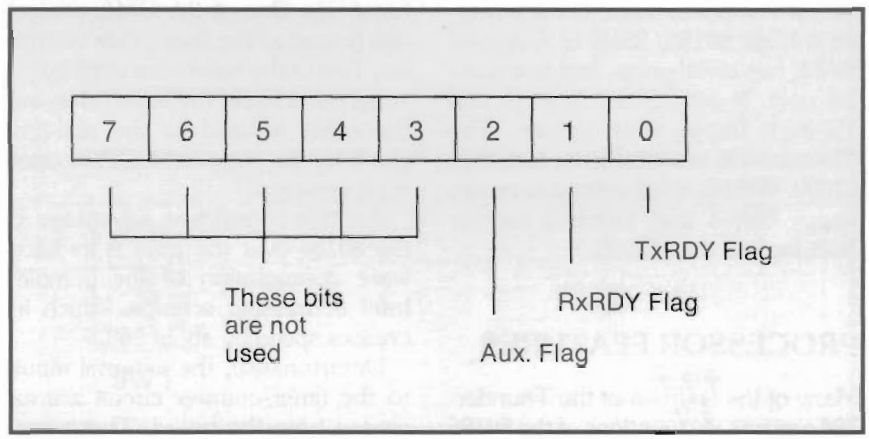


Figure 1. *Slave to Master Status Register Bits.*

SOFTWARE

At the present time, Teletek provides software support for the SBC 86/87 under the TurboDOS operating system. TurboDOS allows a system integrator to assemble a powerful multiuser/multiprocessing system based on Teletek's master, slave, and hard-disk/tape controller boards. The standard TurboDOS implementation of the SBC 86/87 is CP/M-86 compatible. An MS-DOS 1.0 emulator is furnished at no extra cost.

For other applications, Teletek can provide examples of the existing software to aid in the development of new drivers.